

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:

Masaya MURANAKA et al.

Appln. No.:

Filed: HEREWITH

For: METHOD OF DECIDING ERROR RATE AND SEMICONDUCTOR
INTEGRATED CIRCUIT DEVICE

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INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

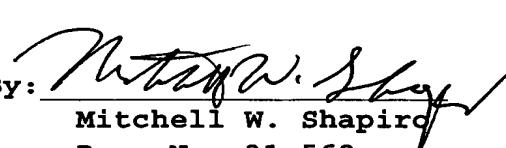
Sir:

Applicants wish to make of record the documents cited
in prior Application No. 09/875,961 filed June 8, 2001,
whether cited by Applicants or by the Patent Office. The
documents are listed on the attached Form PTO-1449.

Respectfully submitted,

MWS:adc

Miles & Stockbridge P.C.
1751 Pinnacle Drive
Suite 500
McLean, Virginia 22102-3833
(703) 903-9000

By: 
Mitchell W. Shapiro
Reg. No. 31,568

March 25, 2004

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| FORM PTO-1449 | | Atty. Docket No. | Appln. No. |
| LIST OF DOCUMENTS CITED BY APPLICANT | | XA-9485A | |
| | | Applicant | |
| | | Masaya MURANAKA et al. | |
| | | Filing Date | Group |
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| Examiner | Date Considered |
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.